







This diagram shows a cross-sectional view of a semiconductor device with two vertical structures. The substrate consists of an n-type region (10) at the bottom, followed by a p-type region (2), and an n+ region (1) at the top. Each vertical structure contains a central n+ region (3) surrounded by a p-type region (8a). The structures are separated by a p-type region (8b). The top surface is labeled 5a, and the bottom surface is labeled 6. The side walls are labeled 7 and 9. The top surface of the substrate is labeled 10.

FIG 2 (PRIOR ART)

FIG 2 is a cross-sectional view of a semiconductor device, labeled as "FIG 2 (PRIOR ART)". The device consists of a periodic array of vertical columns. Each column has a central core (8) surrounded by a layer (9). This core is embedded in a matrix of layers (5 and 5a). The matrix is further divided into regions labeled "n+" and "1". A horizontal line A-A is drawn across the top and bottom of the device, indicating a cross-section.

	Gate		p (channel area)		Isolation/ dielectric
	Webs (AT) (Source region)		Poly Si/ tungsten/WL		Drain region